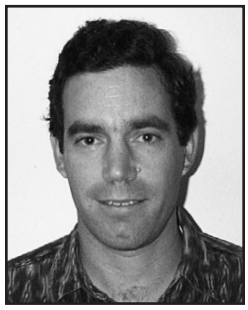
SE3 Analog Scaling



Organizer: Andrea Baschirotto, University of Lecce, Lecce, Italy
Chair: Robert Neff, Agilent Labs, Palo Alto, CA

From ITRS, technology scaling is a robust roadmap for digital circuits, while analog circuits strongly suffer from this trend, and this is becoming a crucial bottle neck in the realization of a SoC in a scaled technology merging high-density digital parts, with high-performance analog interfaces. This is because scaled technologies reduce the supply voltage, and this limits the analog performance in qualitative (is it possible to operate from a low voltage?) and quantitative (if it is possible to operate, which performance is achievable?) terms. In fact the reduced voltage and the modified analog performance of scaled technologies devices imply a lower output swing and a reduced dynamic range for the analog circuits. And this is more and more critical in advanced signal processing systems, which require large dynamic range at low-supply voltage. Analog designers have then to face challenging trade-off between supply headroom, device matching, gain and accuracy, etc.

This Session is organized in three talks, that deal with these critical issues, giving an overview of the present situation and a forecast of the future. Each talk will deal with one of the following open questions:
- How will the new scaled technologies affect the power consumption of an analog system?
- Which analog topologies will be feasible in scaled technologies?
- Which performance will be possible in scaled technologies?

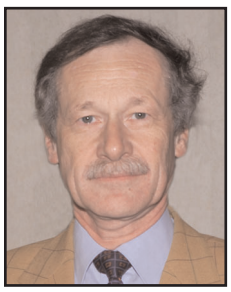
Each presentation will analyze the situation of the different blocks in an analog-signal-processing unit, like gain stages, filters, ADCs, etc.

 1-4244-0079-1/06/$20.00 ©2006 IEEE

Position Statements

The Effect of Technology Scaling on Power Dissipation in Analog CMOS Circuits
Klaas Bult, Broadcom Netherlands, Bunnik, The Netherlands
A general approach for Power Dissipation estimates in Analog CMOS circuits as a function of Technology scaling is introduced. It is shown that as technology progresses to smaller dimensions and lower supply voltages, matching dominated circuits are expected to see a reduction in power dissipation whereas noise dominated circuits will see an increase. As an example of how these results may be used, they are applied to ADC architectures like Flash and Pipeline ADC's and it is shown why Pipeline ADC's survive better on a high, thick-oxide supply voltage whereas Flash ADC's benefit from the technology's thinner oxides. As a result of these calcula-tions an adaptation to the most popular Figure-of-Merit (FOM) for ADC's is pro-posed. Comparisons between published numbers for Power Dissipation and estimates based on the presented theory are presented to show the validity of this approach. Finally, a prediction of future scaling will be discussed, using the latest ITRS predictions on power-supply scaling.

Analog Circuit Solutions in Scaled Technologies
Andrea Baschirotto, University of Lecce, Lecce, Italy
From the ITRS, the technology scaling gives a reduction of the supply voltage sustainable by analog devices and it is accomplished by a reduction of the MOS device threshold voltage. However the threshold voltage reduction is lower than the power supply reduction. The effects of this slope difference in the main building blocks will be addressed. Literature data will validate the concept that in scaled technologies, when the matching noise is non-dominant, the same performance is achieved with a higher power consumption. Finally, for the main analog blocks (like current mirrors, bandgaps, switches, opamps) the possible solutions able to operate at these new conditions driven by the technology scaling will be proposed.



Delta-Sigma Converters in Scaled CMOS Technologies
Willy Sansen, KU Leuven, Leuven, Belgium
In nanometer CMOS technologies, the supply voltage is reduced to below 1 Volt. As a result, the dynamic range of analog blocks, and specifically of Delta-sigma AD Converters is limited by lack of gain and by distortion. Moreover switches have become hard to realize. Specific circuit design techniques are thus required to achieve high dynamic range, at low voltages for low power.

High gain can be achieved by cascodes, gain-boosting, cross-coupling, bootstrapping, current-starving, etc. They will be discussed and compared. The reduction of distortion in Delta-sigma converters at low supply voltages can be realized by means of full-feedforward, switched OTA's, unity-gain reset, input series resistances, etc. They are all discussed in detail and compared in performance.